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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,413	02/28/2002	Brian Tse Deng	TI33539	3213

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,413	DENG ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-9, 12,14,15 and 21-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,11,13 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

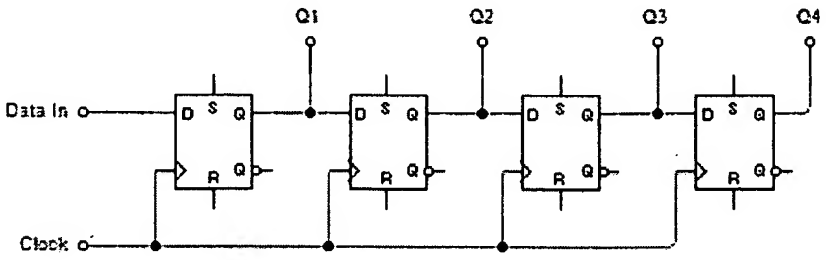
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Norris et al. (Norris, 4,523,104).

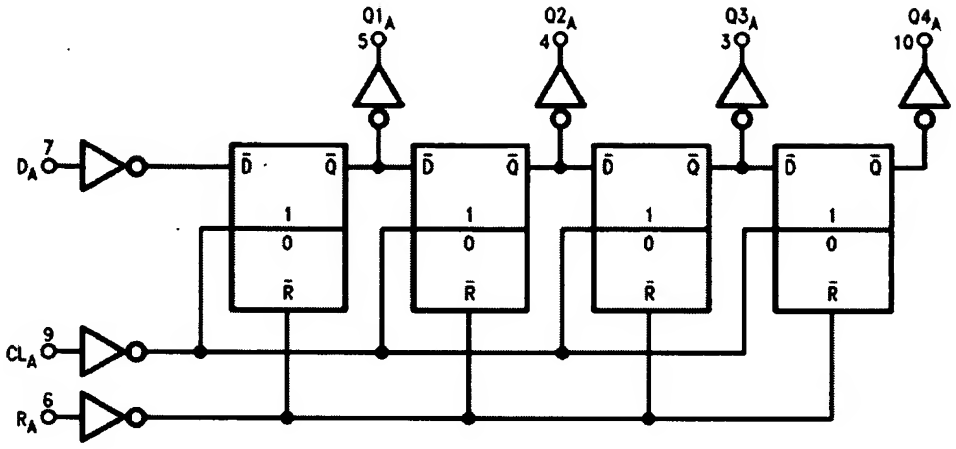
As broadly drafted, these claims do not define any structure that differs from Norris.

With regard to claim 10,Norris discloses a signal debouncing circuit (shown generally at Figs. 1 and 2; the shift register 14 of the debouncing circuit of Norris is a CD 4015 serial in-parallel out shift register. A serial in-parallel out shift register is shown below (see Wikipedia definition of a shift register, cited below):

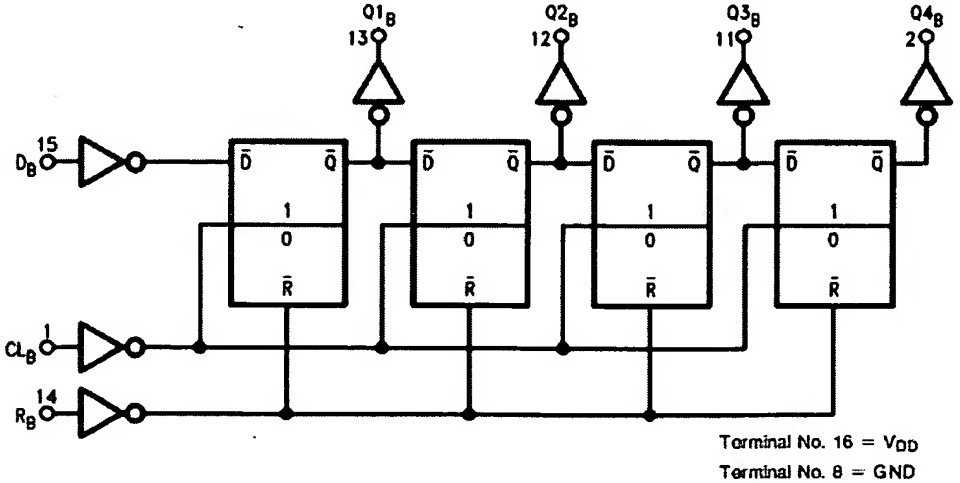


Specifically, the CD 4015 shift register of Norris is show below:

Logic Diagrams



Logic Diagrams (Continued)



(see National Semiconductor, CD4015.)

comprising: a memory device (it is clear from above that the first flip flop of the shift register 14 is readable as a memory device) coupled to a signal line, the memory device to store a value based on a signal value on the signal line (the first flip-flop of the shift register 14 stores a value based on a signal value on the signal line from the switch 12 for storing an input value); a serially connected sequence of storage devices coupled to the memory device (a series subsequent flip flops is readable as a sequence of storage devices connected to the first flip-flop), wherein: an input of a first storage device is coupled to the memory device (the flip-flop adjacent to the first flip flop is readable as a first storage device coupled to the first flip-flop); an input of subsequent storage devices is selectively coupled to an output of a previous storage device (the input of the subsequent flip-flop is selectively coupled to the output of the previous flip-flop); and an output of a last storage device provides a debounced version of the signal value provided to the memory device (it is clear from above that the last flip-flop of the shift register 14 of the debouncing circuit comprises an output to provide a debounced signal originated from the signal value provided to the first flip-flop or "memory device" of the shift register 14 of the debouncing circuit of Norris).

With regard to claim 11, it is clear that the input of subsequent storage devices or subsequent flip-flops are selectively coupled to the output of a storage device immediately before it in the sequence of storage devices (note that the sequence of storage devices are the sequence of flip-flops between the first flip-flop and the last flip-

flop of the shift register 14 of the debouncing circuit of Norris).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

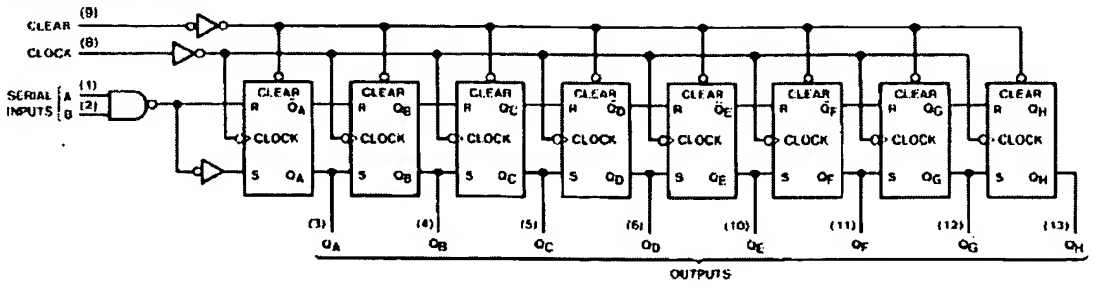
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norris et al. (Norris, 4,523,104).

Norris, as discussed above, discloses the claimed invention except that Norris does not disclose the use of additional flip-flops including the so-called "final storage device."

As noted above, the CD4015 shift register is a 4-bit shift register comprising 4 flip-flops. An 8-bit version of a shift register is shown below (see 8-bit shift register cited below):

Logic Diagram



It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an 8-bit shift register instead of a 4-bit version for the shift register 14 of the debouncing circuit of Norris, since the use 8-bit shift register vs. 4-bit shift register is only a matter of design choice depending on a particular application and a amount of data to be processed; and selecting an 8-bit shift register only involves ordinary skill in the art. As a result, since an 8-bit shift register is used in Norris, the last flip-flop (see diagram above) is readable as a "final storage device" (claim 13). With regard to claim 16, the set of two sequentially connected flip-flops (see diagram above) is readable as a "memory device." With regard to claim 17, it is clear that the flip-flops shown above are D-type flip-flops. With regard to claim 18, it is clear from the diagram above that sequence of storage devices comprising a sequence of flip-flops. With regard to claim 19, it is clear from the diagram above that the flip-flops are D-type flip-flops. With regard to claim 20, it is from the diagram above that the final storage device is a flip-flop.

Response to Arguments

Applicants' arguments filed 8/1/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed.

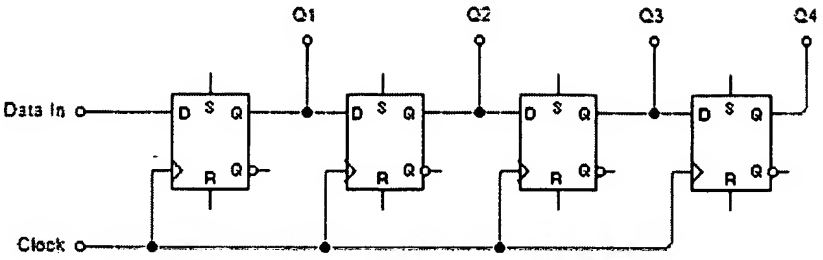
Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 102 Rejection:

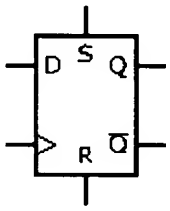
With regard to claims 10 and 11, Applicants argue that "[a]s it is clear from the figures that the examiner has produced in the official action itself, the output of each of the flip-flops of the serial-parallel shift register are directly connected to the output of the previous stage. There is no circuit shown which can provide a selection of whether or not the input to one stage is coupled to the output of another, only a direct hardwired connection, which is not a selection. In view of the fact that '102 rejection must show all the elements of the claim, this rejection should be withdrawn."

Contrary to Applicants' argument, the CD 4015 serial in-parallel out shift register used in Norris comprises a series of D-type flip-flops. By definition, each flip-flop is considered a memory device.



As shown above, each flip-flop is a D-type flip-flop, and an output Q of one flip-flop s connected to an input D of the next flip-flop.

The D-type ("Data") flip-flop takes one input, which it conveys to the output when the clock is strobed. Regardless of the current value of the output, it will assume a value 1 if D = 1 when the flip-flop is strobed or a value 0 if D = 0 when the flip-flop is strobed. This flip-flop can be interpreted as a primitive delay line or zero-order hold, since the data is posted at the output one clock cycle after it arrives at the input. It is called delay flip flop since the output takes the value in the Data-in. The following is a symbol of a D-type flip-flop:



The characteristic equation of the D flip-flop is:

$$Q_{next} = D$$

and the corresponding truth table is:

D	Q>		Q_{next}
0	X	Rising	0
1	X	Rising	1

As already discussed above, these flip flops form the basis for shift registers, which are an essential part of many electronic devices.

It is clear from the definition of D-type flip-flop discussed above, the data D only appears at the output Q after a delay. Further, depending on the strobing of the clock, the D-flip flop takes one input and conveys to an output . As discussed above, the CD 4015 serial in-parallel out shift register used in Norris comprises a series of D-type flip-flops. Each flip-flop is a D-type flip-flop, and an output Q of one flip-flop s connected to an input D of the next flip-flop. Thus, it is clear that depending on the strobing of the clock and after a delay, an input D of each subsequent flip-flop is selectively coupled to an output Q of a previous flip-flop to receive data.

The 103 Rejection:

With regard to claims 13 and 16-20, Applicants argue that the "examiner states that the above noted CD 4015 shift register is a 4 bit shift register comprising 4 flip-flops that an 8-bit version is shown in the action. The examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an 8-bit shift register instead of a 4-bit shift register. However, Applicants did

not understand the significance of the examiner's recitation of an 8-bit shift register instead of the 4-bit shift register, since none of the Claims 13 and 16-20 rejected by the examiner recite an 8-bit shift register."

In response to Applicants' argument, as already discussed, the CD 4015 shift register is a 4 bit shift register comprising 4 flip-flops (a type of memory element). As claimed, claims 13, 16-20 require more flip-flops or memory element. The 8-bit version of the shift register contains more flip-flops than the 4-bit version. Thus, It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an 8-bit shift register instead of a 4-bit version for the shift register 14 of the debouncing circuit of Norris, since the use 8-bit shift register vs. 4-bit shift register is only a matter of design choice depending on a particular application and a amount of data to be processed; and selecting an 8-bit shift register only involves ordinary skill in the art. As a result, since an 8-bit shift register is used in Norris, the last flip-flop (see diagram above) is readable as a "final storage device" (claim 13).

The Restriction:

As discussed in the previous Office Action, at issue is NOT whether the species are "similar" but whether the claims are directed to patentably distinct species. As set forth in the Restriction Requirement, the species of Figs. 5(a, b) and the species of Figs. 6 (A, B) are patentably distinct because of the reasons set forth in the previous Office Action. In addition, the Restriction set forth in the previous Office Action has already made FINAL. Should applicant traverse on the ground that the species are not

patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Relevant Art

Non Patent Literature/Printed documents: Computer Hardware, Lecture 11: Registers, and definition of Flip-Flop from Wikipedia are also cited as relevant art.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner